

# TCXO

PT184A Series

PECL/LVDS

14PIN DIP PACKAGE

## \* PART NUMBERING GUIDE

PT184A - 5 P 10 3 D C - 20.000M

Supply Voltage

5 : 5.0V  
3 : 3.3V

Output

P : PECL  
L : LVDS

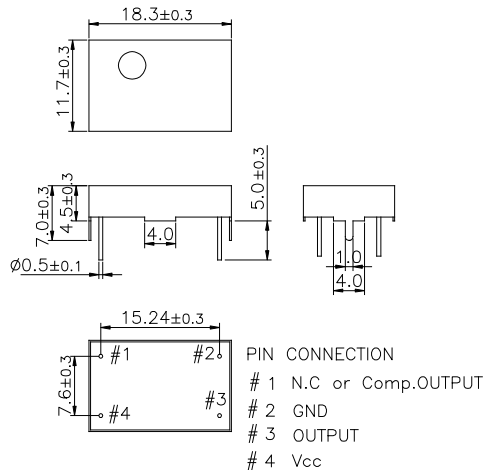
Stability vs. Temperature  
See Table1

Frequency  
M : MHz

C : 1PIN Comp.OUTPUT  
Blank : N.C

Temperature Range  
Table2

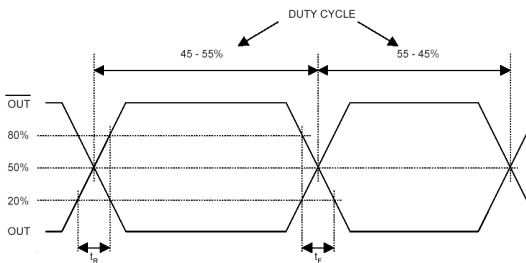
### MECHANICAL DIMENSIONS



### ELECTRICAL SPECIFICATION

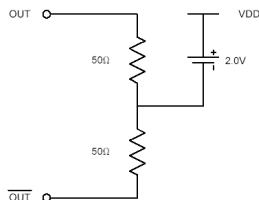
Frequency range	0.75MHz to 800.000MHz All combination of Frequency range Vs. Package type might not be available ,please contact factory.	
Frequency Stability vs. Temperature vs. Supply Voltage vs. Load vs. Aging	±0.5 ppm to ±5.0ppm ±0.1 / ±0.3 ppm max / Vdd ± 5% ±0.2 ppm max /15pF ±10% ±1.0 ppm max/ year	
Temperature Range Operating Storage	See Table 2 -55°C to 125°C	
Supply Voltage	3.3V ± 5% 5.0V ± 5%	
Input Current 3.3 V , 5V	24.000MHz ~ 25mA max	800.000MHz ~ 100mA max
Output characteristics	pecl	lvds
Voh Logic "1"	Vdd-1.025v min.	1.43v typ.
Vol Logic "0"	Vdd-1.620v max.	1.10v typ.
Rise Time Tr	1.0 nsec max.	1.0 nsec max.
Fall Time Tf	1.0 nsec min.	1.0 nsec min.
Duty Cycle	50//50 ± 5%	50//50 ± 5%
Differential Output	Vod(Lvds)	330mV typ.
Offset Voltage	Vos(Lvds)	1.2V typ.
Phase Noise (typical) 20MHz offset	-80 dBc / Hz @ 10Hz -120 dBc / Hz @ 100Hz -135 dBc / Hz @ 1KHz -140 dBc / Hz @ 10KHz -145 dBc / Hz @100KHz	
Frequency Adjustment	±3ppm min by internal trimmer	

### OUTPUT WAVEFORM

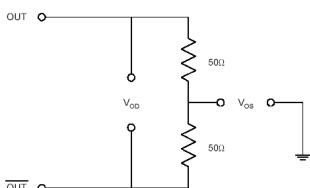


### TEST CIRCUIT

PECL Levels Test Circuit



LVDS Levels Test Circuit



### ENVIROMENTAL & MECHANICAL SPECIFICATION

Shock	MIL-STD-883C, Method 2002, Condition B
Vibration	MIL-STD-883C, Method 2007, Condition A
Solderability	MIL-STD-883C, Method 2003
Seal integrity	MIL-STD-883C, Method 1014, Condition C & A2
Marking	MIL-STD-202F, Method 215

#### TABLE1

Symbol	Stability
05	±0.5ppm
10	±1.0ppm
15	±1.5ppm
20	±2.0ppm
25	±2.5ppm
30	±3.0ppm
35	±3.5ppm
50	±5.0ppm

#### TABLE2

Symbol	Temp.	Symbol	Temp.
0	0°C	A	50°C
1	-10°C	B	60°C
2	-20°C	C	70°C
3	-30°C	D	75°C
4	-40°C	E	80°C
		F	85°C